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A SURVEY OF ANALOG-TO-DIGITAL CONVERTER TECHNOLOGY FOR RADAR APPLICATIONS

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29 MARCH 1982

U.S. ARMY MISSILE COMMAND
Redstone Arsenal, Alabama 35898

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20. ABSTRACT *(Continue on reverse side if necessary and identify by block number)*

The first section of this report discusses sample-and-hold devices (SHD) which are required prior to the analog-to-digital converter (ADC) in most radar applications. The SHDs discussed had acquisition times of 10 μsec or less. Plots of SHD droop rate and aperture uncertainty versus acquisition time are presented. The next section contains details on a variety of commercial off-the-shelf ADCs that have sampling rates greater than 100 KHz.

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20. Abstract (Continued)

They are compared by resolution, sampling rate, packaging, logic family, size, cost, power requirement, and temperature stability. Finally, brief descriptions of ADCs in development are discussed, and a resolution versus sampling rate comparison of non-commercial ADCs being manufactured by radar houses and their suppliers is presented. The performance envelopes of the commercial and non-commercial ADCs are then overlayed on the estimated 1988 Radar and ELINT resolution and sampling rate requirements.

CONTENTS

ACKNOWLEDGMENTS

The author acknowledges Drs. Don Burlage and Eugene R. Billiam, whose 1978 report "Survey of Analog-to-Digital Converter Technology for Radar Applications," prepared for the Technical Co-Operation Program Subgroup KTP-3 is updated by this report.

I. INTRODUCTION

Continuing advances in digital technology for application to radar signal processors are placing an increasing burden on the conversion of analog video signals to digital signals. Operating speeds and storage densities of digital logic are increasing to such a degree that the processing of wider video bandwidths and dynamic ranges, respectively, is beginning to be limited by the sampling rates and bits of resolution available in Analog-to-Digital (A/D) converters. This paper is an attempt to assess the limitations on the state-of-the-art of A/D Converter technology and determine the potential for near-term improvements.

Information on A/D converter technology was obtained by contacting over 237 manufacturess by letter in Canada, the UK, and the US, by discussions with radar manufacturers and by reviewing other A/D converter surveys. From these contacts, the 26 manufacturers listed in Table 1 provided information on A/D converters suitable for radar applications with a 100 KHz or greater sampling rate. While there were a number of suppliers that did not respond to the survey, there were 51 manufacturers that responded with data on A/D converters with sample rates less than 100 KHz, syncro-to-digital resolvers, voltage-to-frequency converters, or delta modulators none of which were included in the investigation.

TABLE 1. SUPPLIERS OF A/D CONVERTERS APPLICABLE TO RADAR*

1. ADAC Corp	10. HYBRID Systems	19. Preston Scientific
2. Analog Devices	11. ILC Data Device Corp	20. RCA
3. Analogic	12. Intech	21. Teledyne Philbrick
4. Burr-Brown	13. LeCroy	22. TRW LSI Products
5. Computer Labs	14. Micro Networks	23. TRW Electronic Systems
6. Datel-Intersil	15. Mostek	24. Westinghouse
7. Dynamic Measurements	16. Phoenix Data	25. Zeltek
8. Ferranti	17. Plessey	26. Motorola
9. Hughes Aircraft	18. Precision Monolithics	

*These numbers will serve as the key to suppliers on the graphical summaries presented in this paper.

The first section of this report is concerned with sample-and-hold devices (SHD) which are required prior to the A/D converter in most radar applications due to the relative bandwidth of the signals being digitized and the conversion speed of the A/D converter. Such a device ideally is needed to instantaneously sample the video voltage and hold it at a constant level while the A/D converter accurately converts the voltage to a digital representation. Errors and limitations of available SHD's are presented. The next section, which is the emphasis of the paper, contains details on the variety of available off-the-shelf A/D converters. They are compared by resolution, sampling rate, packaging, logic family, size, cost, power requirement, accuracy and temperature stability. Finally, following the two sections on commercially available devices are brief descriptions of the A/D converters in a developmental status.

II. SAMPLE AND HOLD DEVICES

The Sample-and-Hold Device (SHD) in its basic form consists of a switch followed by a capacitor. When the switch is closed under control of a sample command, the SHD output will follow the changing analog input signal until a hold command occurs. At this time, the switch will open and the device will hold the voltage on the capacitor subject to capacitor and switch leakage. Input and output amplifiers and other sophisticated circuity are employed to minimize switching and leakage effects. However, a number of SHD errors must still be considered.

Important SHD parameters are illustrated in Figure 1 which shows a typical input signal and the resulting error sources. The acquisition time, which is the length of time after the sample command until the output is tracking the input within some specified accuracy, is a basic limitation on the conversion cycle time of the SHD/A/D converter cascade. Acquisition time must be significantly less than the desired cycle time to leave time for the analog-to-digital conversion during the hold mode. The other two errors illustrated are limitations on A/D converter accuracy. Aperture time is the length of

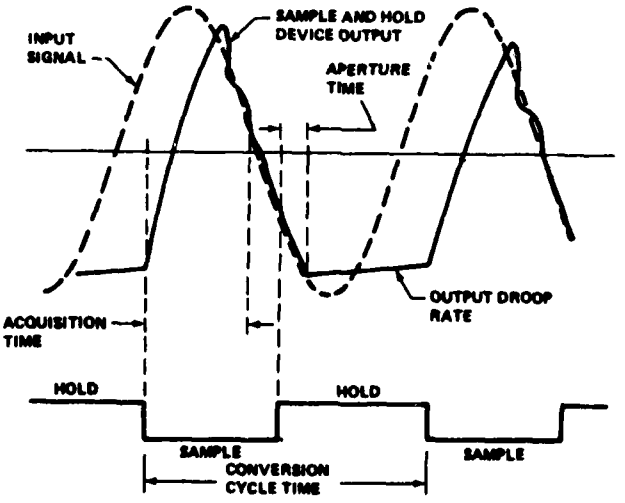

Figure 1. Effect of Sample and Hold Parameters on Output Waveforms.

time between the hold command and the time when the sampling switch is completely open. This time delay is not an error source itself since it can be eliminated by applying an early hold command if the delay is constant from cycle to cycle. Unfortunately, it is not constant and the resulting variation between the minimum and maximum aperture time to be expected is defined as the aperture uncertainty time. This time variation results in a voltage uncertainty at the SHD output. Another voltage error at the output is due to the leakage of the capacitor voltage during the hold mode. A parameter defined as the output droop rate, usually in mV/msec, is used to specify this error.

The aperture uncertainty and output droop rate for available SHD's are given in Figures 2 and 3 as a function of the device acquisition time. Numbers under each point correspond to the appropriate supplier listed in Table I and the symbol indicates the SHD package, i.e., Dual-In-Line Package (DIP) or module. The DIP's are either monolithic or hybrid integrated circuits and the modules are either Printed-Circuit (PC) boards or potted circuits. Burr Brown and Micro Networks, do not provide aperture uncertainty values for some of their SHD's; however, their marketing offices provided an estimate. All output droop rates were not available. Consequently, for a few points on Figure 2 there won't be a corresponding point plotted on Figure 3.

There are easily recognizable patterns on the error curves, namely, fast acquisition times correspond to both low aperture uncertainties and high droop rates. Conversely, the slow devices have high uncertainty errors but better droop characteristics. These tradeoffs result from a compromise that must be made during the capacitor hold circuitry design, i.e., large capacitance limits the slewing rate during acquisition but a small capacitance has larger droop characteristics. For the modern radar which might require a 10 MHz A/D conversion rate, the corresponding cycle time to 100 nsec limits the SHD selection to only a few devices. Fortunately, many of the high performance A/D converters for radar are supplied with an internal SHD eliminating the selection problem. For example, the Computer Labs 25 nsec acquisition time SHD is used internally in the construction of their 5 and 10 MHz converters described in the next section.

III. ANALOG-TO-DIGITAL CONVERTERS

The majority of A/D converters for radar applications employ either the successive-approximation technique, the parallel flash technique or an iteration or a variation of either technique. These techniques are discussed briefly in this section but the converter specifications are described in more detail.

A. Implementation Consideration

The successive-approximation converter compares the unknown input voltage with a quantized estimate of the input and successively changes bits of the estimate until the difference between the two is within a voltage quantum corresponding to the Least-Significant-Bit (LSB) of the converter. In order to make the comparison, a high precision Digital-to-Analog Converter (DAC) is used to convert the binary estimate to an analog voltage which is subtracted from the unknown input in an analog comparator circuit. The polarity of this error voltage controls which bits of the binary estimate are changed at each successive step in the approximation.

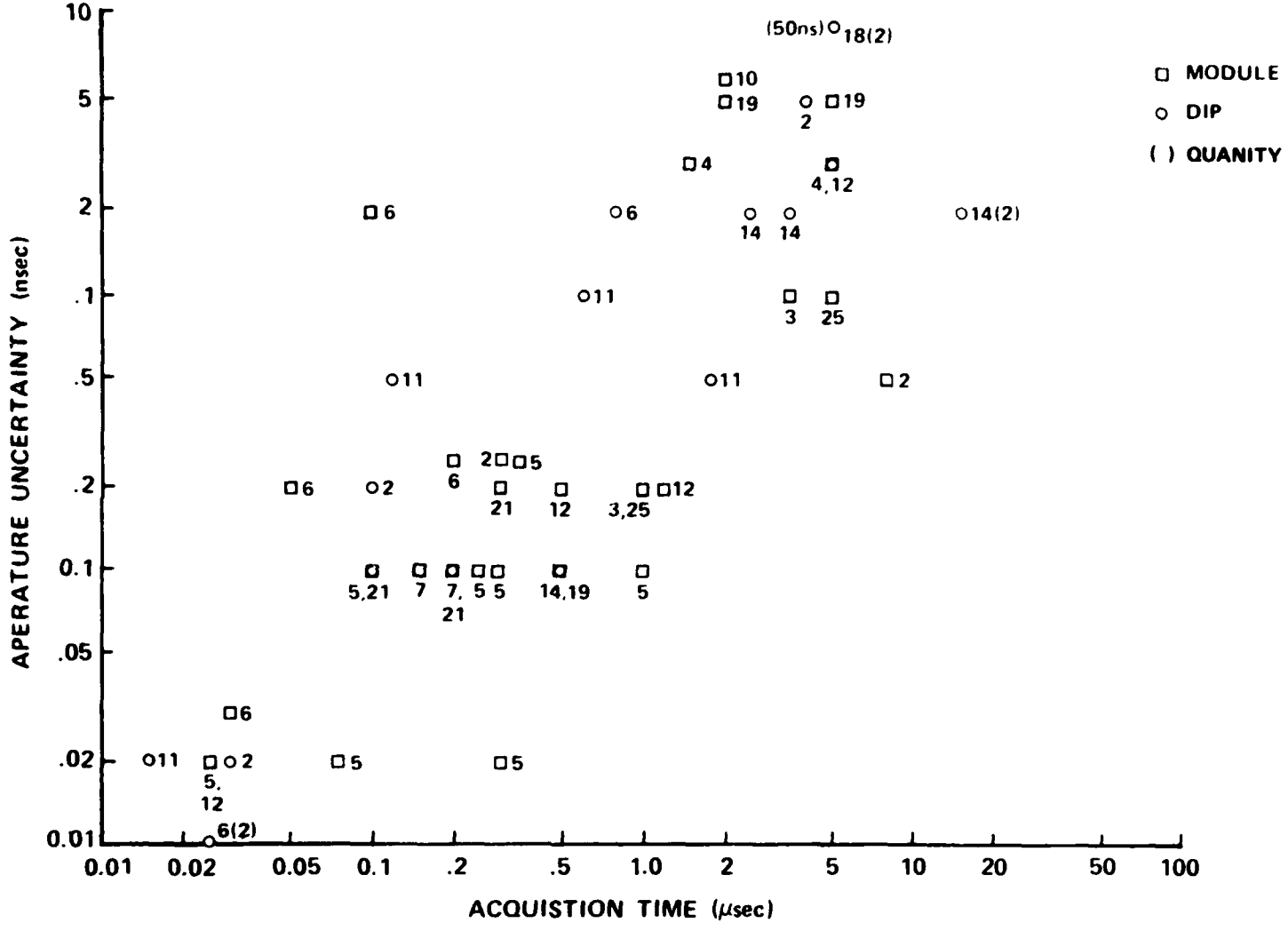

Figure 2. Sample and Hold Aperture Uncertainty.

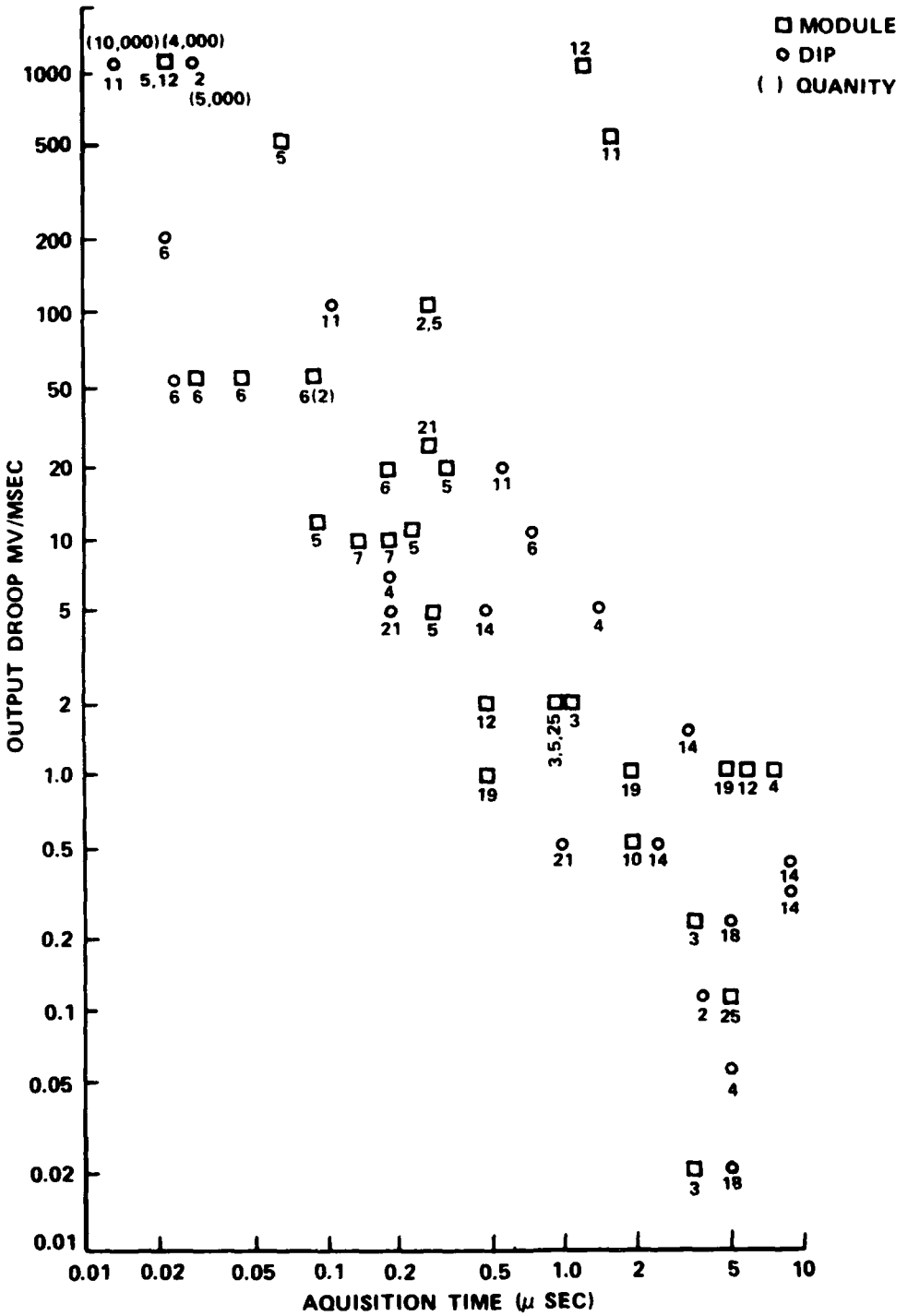

Figure 3. Sample and Hold Output Droop Rate.

The parallel-approximation technique, sometimes defined as the flash approach, is a simultaneous conversion which employs (2^N-1) analog comparators, where N is the number of bits of desired resolution. The unknown input voltage is applied to each comparator with the other input being a precision reference voltage. The (2^N-1) reference voltages correspond to the (2^N-1) switching points between the voltage extremes of the A/D converter rated input range. Consequently, for any unknown input, only one set of adjacent comparators will exist with one having its reference voltage exceeding the unknown and the other having the unknown exceeding the reference voltage. The location of this pair directly defines the output binary estimate.

Of the two types, the successive-approximation converter inherently has a slower conversion time which increases as the resolution increases. As a result, the use of a SHD is imperative for high resolution, successive-approximation conversion of wide bandwidth signals. On the other hand, the parallel cnversion is so fast that recently developed parallel converters do not require SHD's for a significant bandwidth of input signals. The problem with this technique, however, is that the number of comparators, reference voltages and interconnections increases exponentially as the resolution in bits increases.

These tradeoffs between speed and resolution requirements have resulted in many converters using a combination of the two techniques. The so-called serial-parallel, or subranging ADC's, employ at least two parallel ADC stages, a DAC, and an analog subtractor. The first M most-significant bits of conversion are determined in parallel using one of the parallel stages, then with the M-bit DAC this voltage is subtracted from the unknown input voltage, and the second parallel stage is used to convert the difference voltage to obtain the L least significant bits. This technique significantly reduces the amount of parallel hardware required while maintaining stage delays at a minimum. For an 8-bit converter, this technique requires only 30 comparators (15 per stage) as opposed to 255 for an all-parallel case. However, advances in integrated circuit fabrication have made 8 and even 9 bit (requiring 511 comparators manufactured by TRW) parallel converters available in a dual-in-line packages.

B. Comparison of A/D Converter Resolution, Speed, and Packaging Considerations

As discussed above, the design of an A/D converter involves a tradeoff between resolution and speed. Since modern radar systems require both resolution and speed, it is apparent that A/D converter selection for radar applications is not a simple task. Presented in Figures 4, 5, and 6 are graphical representations of this resolution and speed tradeoff for three classes of A/D converters.

In the first class, Figure 4, are converters constructed with monolithic or hybrid integrated circuit technologies and packaged in dual-in-line packages. Device technologies CMOS, TTL and ECL are represented. Devices range from 0.1 MHz, 12 bit, TTL, hybrid, successive approximation A/D converter to a 100 MHz, 6 bit, ECL, monolithic, parallel A/D converter. On the balance more than half of the devices operate at sampling rates at or above 1 MHz. In most cases, additional circuitry such as SHD's, and buffer amplifiers, as well as power supplies are required. However, because of their compact dual-in-line

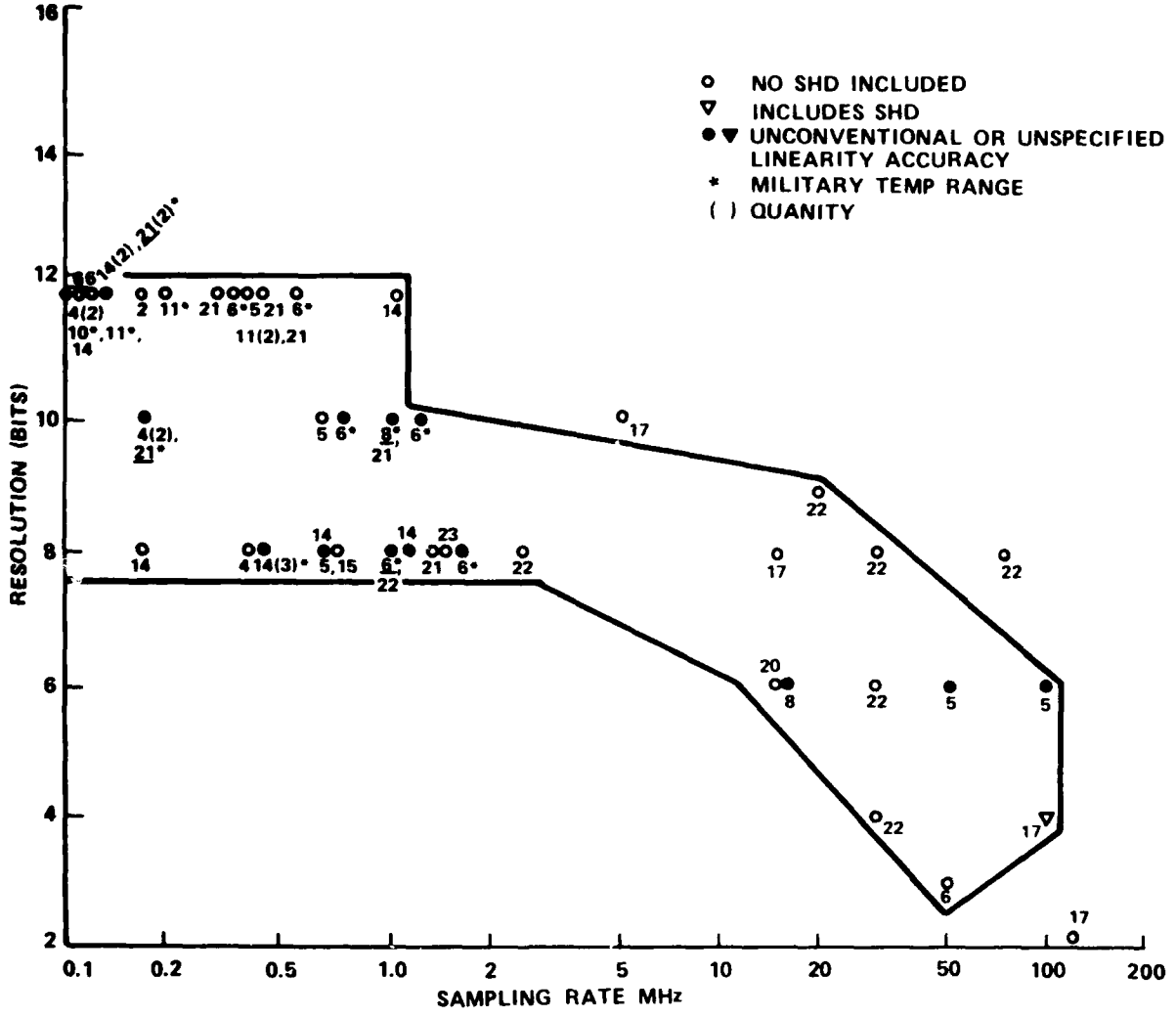

Figure 4. Monolithic and Hybrid A/D Converters.

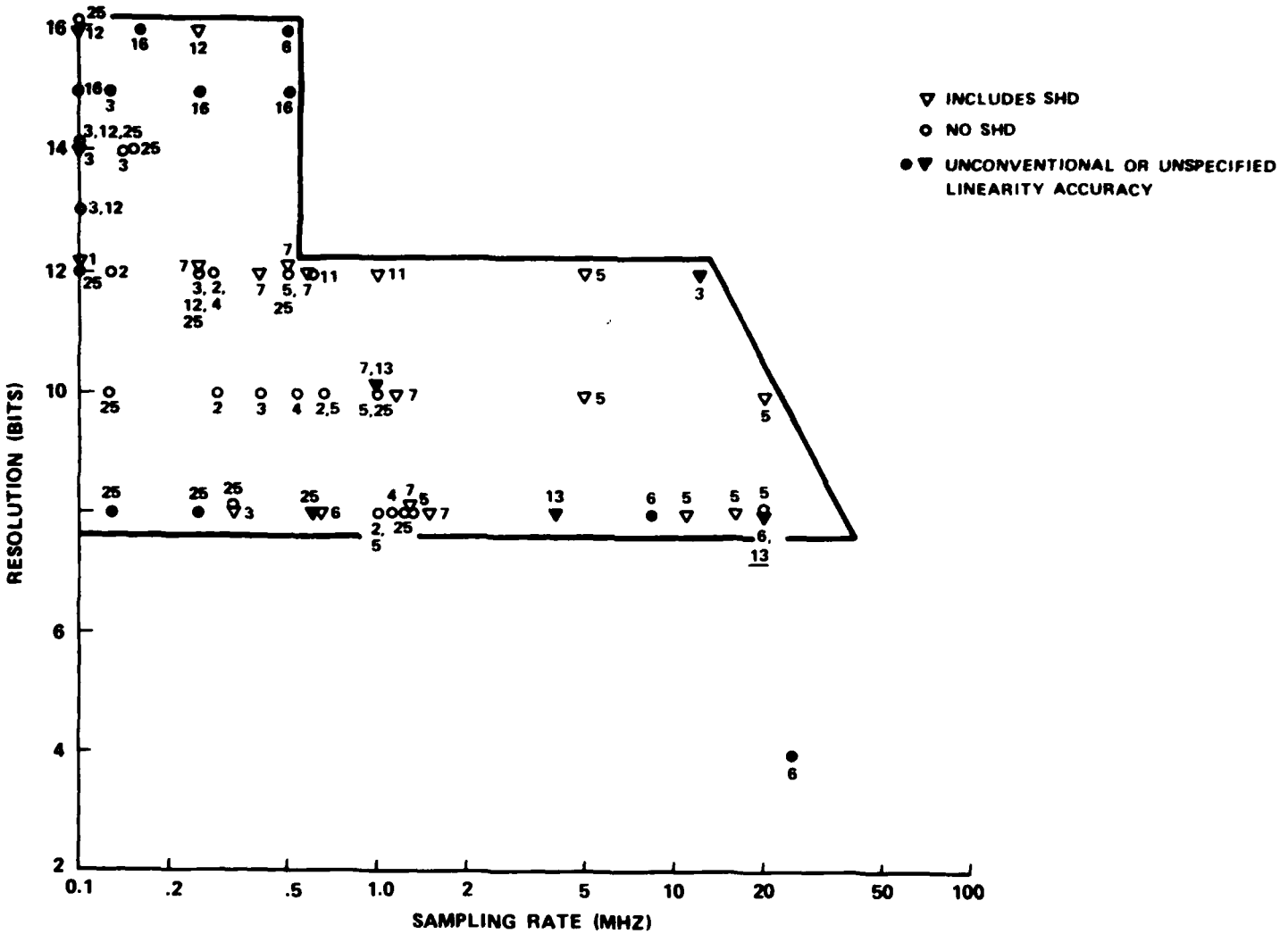

Figure 5. Modular A/D Converters.

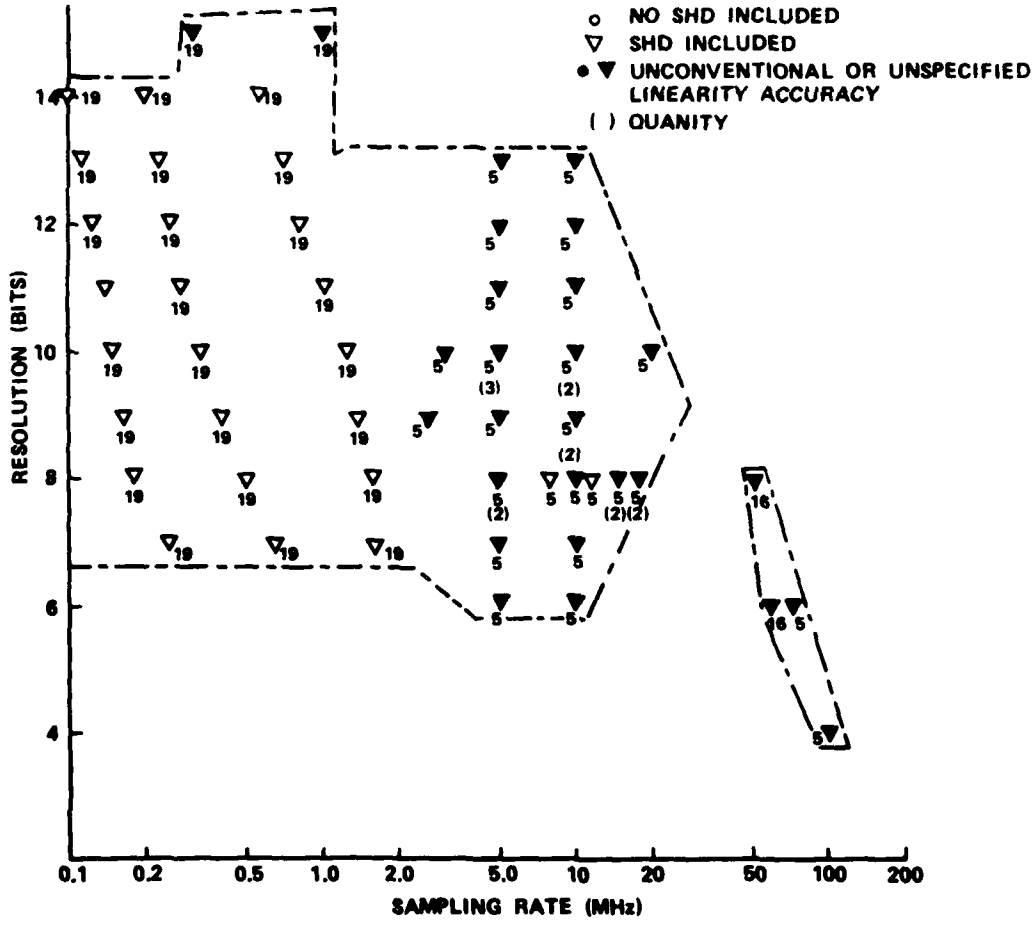

Figure 6. Discrete A/D Converters.

packaging they have a definite potential for radar systems especially in airborne applications such as missile seekers. Another advantage is their close connection with the exploding high-volume field of microprocessor technology. Developmental funds are being invested into this class of converters because of their commercial appeal and these same high-volume applications are expected eventually to reduce their cost similarly to the history of microprocessor devices. Fifty-six devices are in this category as opposed to 29 three years ago.

The modular class of converter in Figure 5 contains the largest variety of devices and manufacturers of any of the three classes. The technologies of ECL and TTL were represented in the converters surveyed. There are a number of low resolution (4 and 8 bit) A/D converters with high sampling rates and a number of high resolution (13 to 16 bits) converters with sampling rates less than 1 MHz. However, modular converters still aren't in abundance at the popular radar requirements of 5 to 10 MHz sampling rates and resolutions of 8 to 13 bits; however, this survey found 11 devices in this range with four of these having either 10 or 12 bit resolution as opposed to 7 total previously.

The last class, the rack-mounted discrete component A/D converter assemblies and subassemblies of Figure 6, provides the widest variety of converters for radar applications. Most of these are complete converters, i.e., power supplies, buffer amplifiers, sample-and-hold devices, and, in some converters, built in test equipment. The Computer Labs A/D converters dominate the 5 to 10 MHz range of sampling rates and, as a result, seem to be the prevalent supplier of commercial ADC's for radar applications. It should be noted, however, that A/D converters developed by radar manufacturers in-house specifically for their systems do not appear on these commercial product charts.

The bounds on resolution and sampling rates for each class of converters are superimposed in Figure 7*. By comparing the classes in pairs, an insight can be gained as to the relative merits of each. For example, DIP converters can replace modular devices except for the high-resolution, low-speed region (A) (where the modular and PCB converters dominate all types) and the medium-resolution, high-speed region (B). Similarly the modular converter can replace the discrete converter assemblies except for 13 bit resolution above 0.5 MHz region (C). The monolothic and hybrid DIP converters clearly dominate in the low-resolutions, high-speed region (D) although some discrete assemblies are available near 100 MHz.

C. Comparison of A/D Converter Cost, Size, Power and Accuracy Considerations

The cost ranges of commercial A/D converters are illustrated in Figure 8 for the three packaging classes as a function of sampling rate. The individual numbers on the cost chart in this case do not refer to manufacturers but are the converter bits of resolution. As would be expected, the DIP products are the most economical, ranging from $40 to $750 in single quantity lots. Modules that overlap the DIP's in performance are approximately in

*No attempt has been made to verify any specifications stated in this survey. In some cases, typical parameters are even compared against minimum performance numbers because of a lack of data on specification sheets.

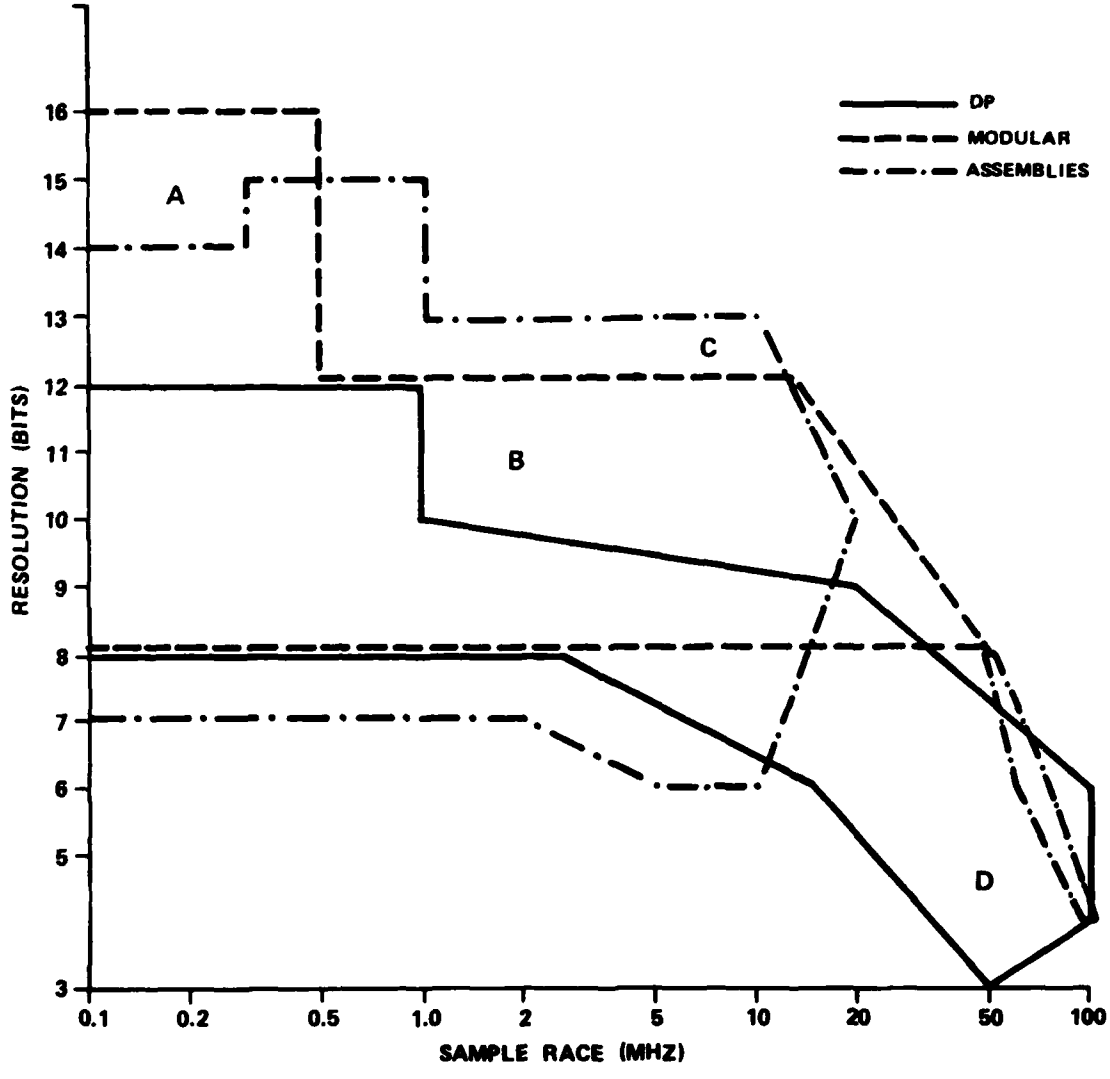

Figure 7. A/D Converter Performance Bounds.

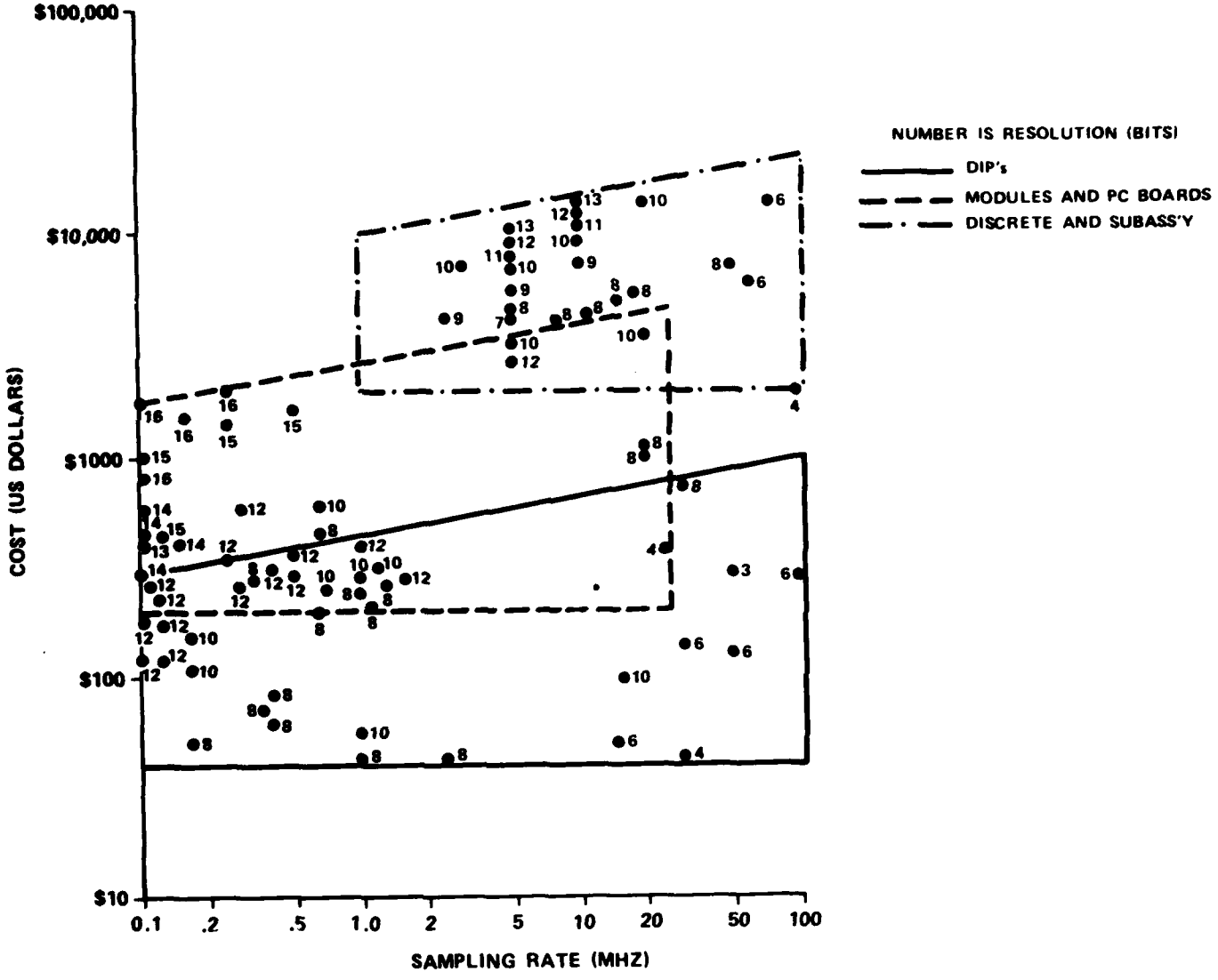

Figure 8. A/D Converter Cost Bounds.

this same price range. The minimum price for modules is about $200 with prices extending to about $4000. The price of discrete converters assemblies start at about $2000 and extend to about $14,000. Prices in all groups increase with sample rate and resolution. Generally low-speed, medium-resolution, and high-speed, low-resolution devices form the price floor.

The size and power requirements of the previously discussed converters are summarized by the ranges given in Table 2. There is nothing unexpected in the range of sizes or in power consumption. The ECL converters were the most power consuming followed by TTL then CMOS. The ECL monolithic devices were mainly found in the non commercial catagory. For all classes and logic

TABLE 2. RANGE OF A/D CONVERTER SIZE AND POWER REQUIREMENTS

		DIP	Modular	Discrete
Size	Volume	0.7-6.4 cm^3	15.2-2058 cm^3	1420 cm^3 -0.065 m^3
	Package Type	16-40 pin DIP	Module or DIP's and/or modules on PC card	PC card subassembly or rack mounted assembly
Power	CMOS	1.5 to 180 mW	--	--
	TTL	0.4 to 3.0 W	0.5 to 18.5 W	36 to 110 W
	ECL	0.45 to 3.9 W	10 to 42 W	25 to 145 W

families the A/D converter with the lowest resolution/ speed product had the lowest power requirement and the highest product had the highest power requirement.

The absolute accuracy of an A/D converter is defined as the difference between the theoretical analog input required to produce a given digital output code and the actual analog input that produces the same code. Three error sources that cause this difference are gain error, offset error, and nonlinearity error. The gain error is defined as the difference in slope between the actual input/ output transfer function relationship and the ideal characteristic whereas the offset error, sometimes called zero error, is the displacement of this transfer function from the origin along the analog input axis. In most converters, these two errors can be adjusted to zero leaving only the nonlinearity error. Nonlinearity is the deviation of the actual transfer function from a straight line drawn between the end points of the input/output transfer function. When the gain and offset errors are zero, the nonlinearity error is often defined as relative accuracy. Since a nonlinear transfer will result in the generation of signal harmonics, especially clutter harmonics, this A/D converter error is one of the more important. The maximum nonlinearity deviation is normally specified to be within $\pm$ 1/2 LSB at 25^{o}C and most A/D converters in this survey met this specification.

One other accuracy specification of importance is differential nonlinearity, defined to be the deviation from 1 LSB of any quantum interval, or "step," in the transfer function. Ideally, the differential nonlinearity is zero. If the differential nonlinearity error is greater than $\pm$ 1 LSB, at least one quantum interval is greater than 1 LSB in width, then a digital output code will be missing. Some manufacturers indicate no missing codes over the temperature range by specifing "guaranteed monotonic" or "guaranteed no missing codes". Most A/D converters in the survey met this specification, although some only met it at 25°C. Converters that were quoted as having either a relative accuracy error of greater than $\pm$ 1/2 LSB, a differential nonlinearity error of greater than $\pm$1 LSB or if neither error was specified then the device is indicated with shaded symbols in Figures 4, 5 and 6. When more than one manufacturer number is associated with a shaded symbol, the manufacturer's code of the high error A/D converter is underlined. An important conclusion that can be drawn from accuracy specifications on these charts is that 14, 15, and 16 bit converters are less likely to meet the normal linearity error criteria than are the lower resolution devices.

Data on accuracy specifications are usually presented as room temperature values. Only a few A/D converters specified the temperature coefficients over the full military temperature range (-55 to 125°C). These devices are marked with an * on Figures 4, 5, and 6. Finally, temperature stability coefficients are the accuracy parameters of interest. In general, temperature specifications are expressed in parts-per-million of the full scale input voltage per °C (PPM/°C), the percent of full scale/°C, or as a fraction of $\pm$1 LSB /°C. Tabulated in Table 3 are the gain, offset and linearity temperature coefficients, illustrating the range of values found quoted. To use the temperature parameters, 25°C is subtracted from or added to the highest or lowest operating temperature respectively, to be expected in the application of interest. The difference or sum is multiplied by these coefficients and added to the 25°C error numbers.

TABLE 3. TEMPERATURE STABILITY PARAMETERS

	Gain Tempco (PPM/°C)	Offset Tempco (PPM/°C)	Nonlinearity Tempco (PPM/°C)	Monotonic & No Missing Codes Over Temp Range
Best ADC's	$\pm$10 to $\pm$30	$\pm$7 to $\pm$25	$\pm$2 to $\pm$5	-55°C to 125°C
Worst* ADC's	$\pm$30 to $\pm$50	$\pm$25 to $\pm$50	$\pm$5 to $\pm$40	0°C to 50°C

*Except for those that did not satisfy the $\pm$1 LSB differential nonlinearity limit even at 25°C.

Other significant A/D converter parameters are input voltage ranges and output digital codes, but no attempt was made to tabulate either of these. On

many converters these are options and, as a result, any individual A/D converter on the summary charts might be available with two or three input voltage ranges and a similar number of output codes. Input ranges available were typically 0 to 1, 2.5, 5, 10, or 20 V (or the inverse polarities, e.g., 0 to -1 V) for the unipolar devices and ±1, ±2.5, ±5, ±10 V for bipolar inputs. Outputs codes included binary, offset binary, two's complement binary, inverted binary and others. Converters with binary-coded-decimal outputs were the only ones deleted from the charts since this code normally is not compatible with radar processors.

IV. NONCOMMERCIAL A/D CONVERTERS

The A/D converters of most interest to this investigation were not those on the open-market, but ones in development or in military systems. Although it is difficult to obtain detailed specifications on these types of devices, an attempt was made to at least determine the trends of converters in a developmental status. Resolution and sampling rates of A/D converters known to be in some stage of development are illustrated in Figure 9. In the commercial field, there are further developments of converters for waveform recorder applications of 10 bits at 20 MHz and 8 bits at 100 MHz.

One A/D converter development program is currently being funded by the US Department of Defense. Its objective is to develop high speed converters using GaAs technology. Since the contract just began in the fall of 1981 there is no progress to report. However, one of the products of the contract proposal phase was Figure 10. This figure presents the projected 1988 A/D converter resolution and sampling rate requirements for radar and electronic intelligence applications (ELINT). It also compares these requirements to the 1978 Production radar requirements. The 1988 requirements are predicted to increase by about an octave at 15 bits to an order of magnitude at 6 bits for the most demanding radars and almost two orders of magnitude for the most demanding ELINT hardware. An assessment of how well devices currently available or in development will satisfy the projected requirements may be obtained from Figure 11, which superimposes the three commerical and the noncommerical performance envelopes on the projected requirements.

The surprise comes from the DIP performance envelope, which has greatly extended in the low resolution region since 1978. However, it does not extend into the projected 1988 requirements. The discrete converter assembly envelope overlaps projected requirements in the 10 to 13 bit resolution region and the modular envelope overlays them in the 9 to 12 bit region. Devices in development fully satisfy the 8 to 10 bit requirements and satisfies most radar requirements down to the 5 bit region. However, the most demanding 4 to 8 bit applications must continue to wait for A/D converter hardware developments, as also must the projected high resolution 14 to 15 bit applications.

Motorola Inc, Government Electronics Division, Scottsdale Arizona, is developing an emitter-coupled-logic successive approximation 10 bit, 40 megasample per sec A/D converter that could also be operated as an 8 bit, 50 megasample per sec converter. A high speed 8 to 1 and 16 to 1 multiplexer is being tested which could be used with this A/D converter. Motorola is also developing, with discrete parts, a medium resolution (4 to 8 bits) 100 Mhz A/D converter using a one bit feed-forward pipeline architecture. The device is

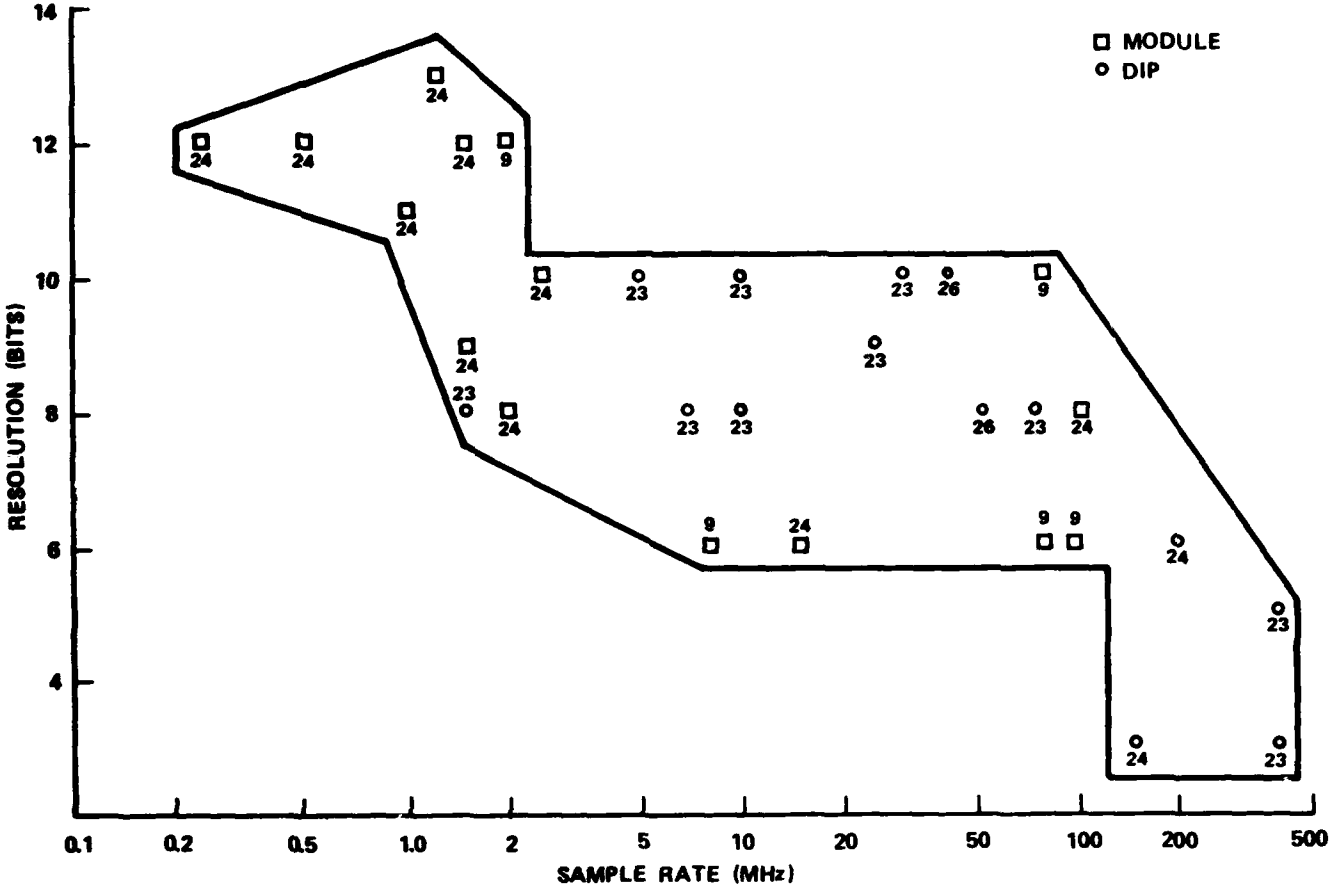

Figure 9. Non Commercial and A/D Converters in Development.

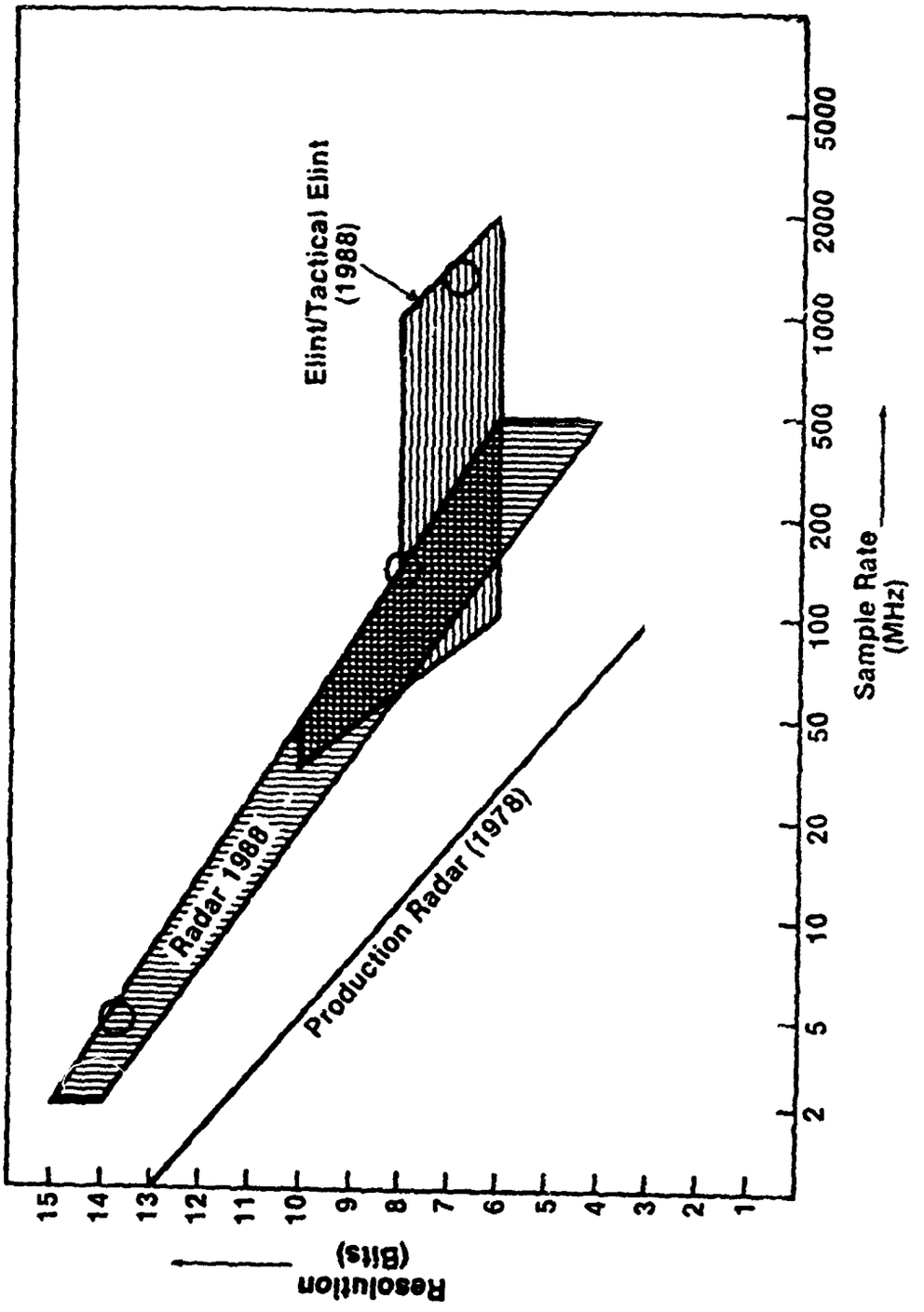

Figure 10. A/D Performance Requirements for 1980s
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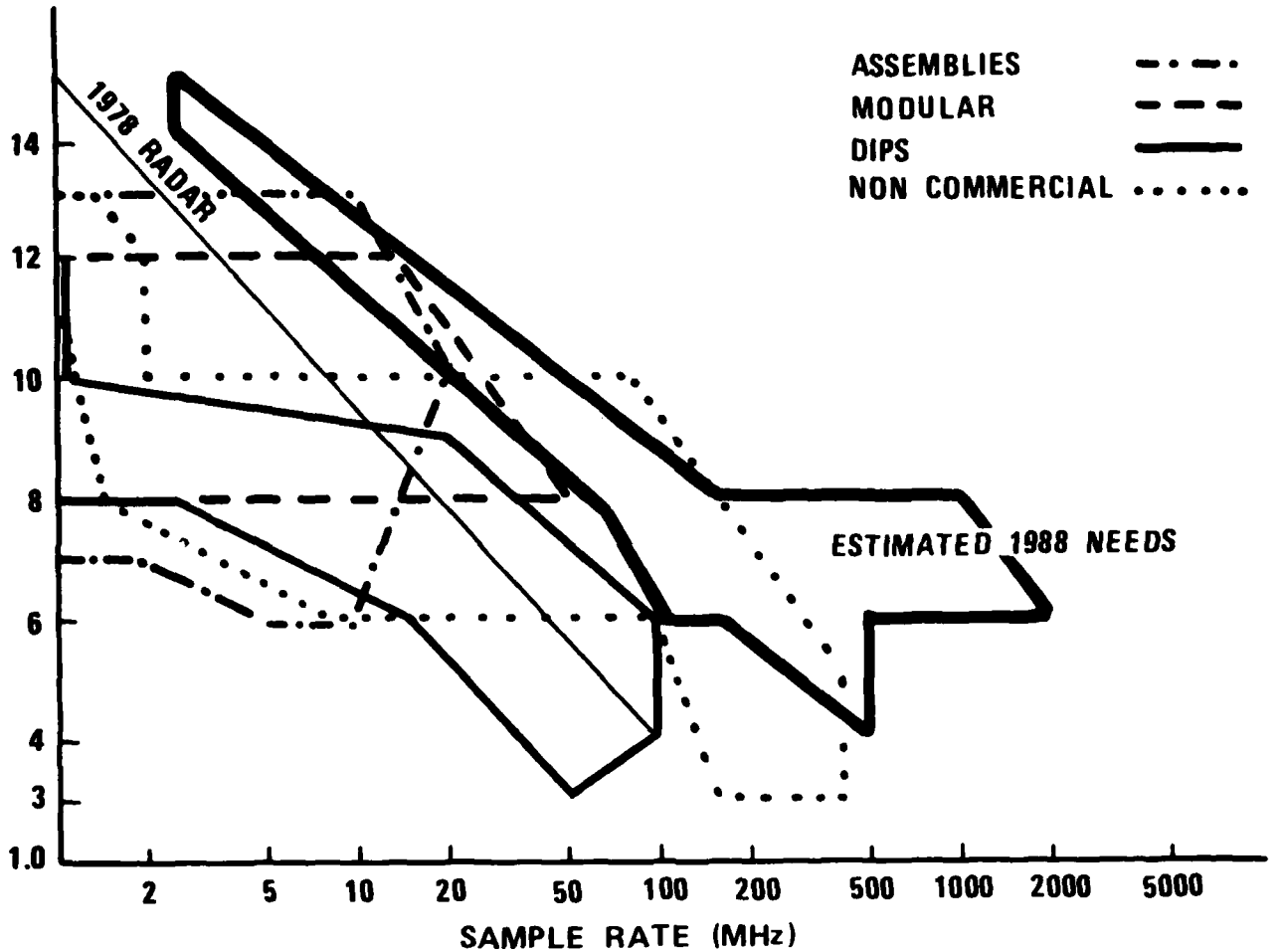

Figure 11. Current Performance and Projected Requirements.

designed to be connected before detection where signal statistical properties will allow certain A/D converter stages to be AC coupled. When GaAS FET transistors were used, the sampling rate was extended to 1000 MHz.

Hughes Aircraft Company, Los Angeles, CA, is working to extend their A/D converter building block resolution to 12 bits and the sampling rate to 250 MHz at lower resolutions. They are using dielectrically isolated emitter-coupled-logic technology and a 5 bit quantizer as a basic element. Hughes is also working to develop an A/D converter using GaAs technology. Their progress with GaAS to date is limited to design, simulation, manufacture, test and evaluation of a comprehensive test circuit and some critical components.

Harris Corporation, Melbourne, FL, is developing a 16 bit 50 KHz monolithic successive approximation A/D converter. The digital-to-analog converter portion of the design has been successfully demonstrated with a settling time of 2 usec. A paper on this design effort is scheduled for presentation at the International Solid State Circuits Conference in 1982.

Westinghouse, Defense and Electronic Systems, Baltimore, MD, is developing an 8-bit 100 MHz A/D converter on a printed circuit board. The converter will be coupled with memory and a microprocessor controller for autocalibration and fault detection.

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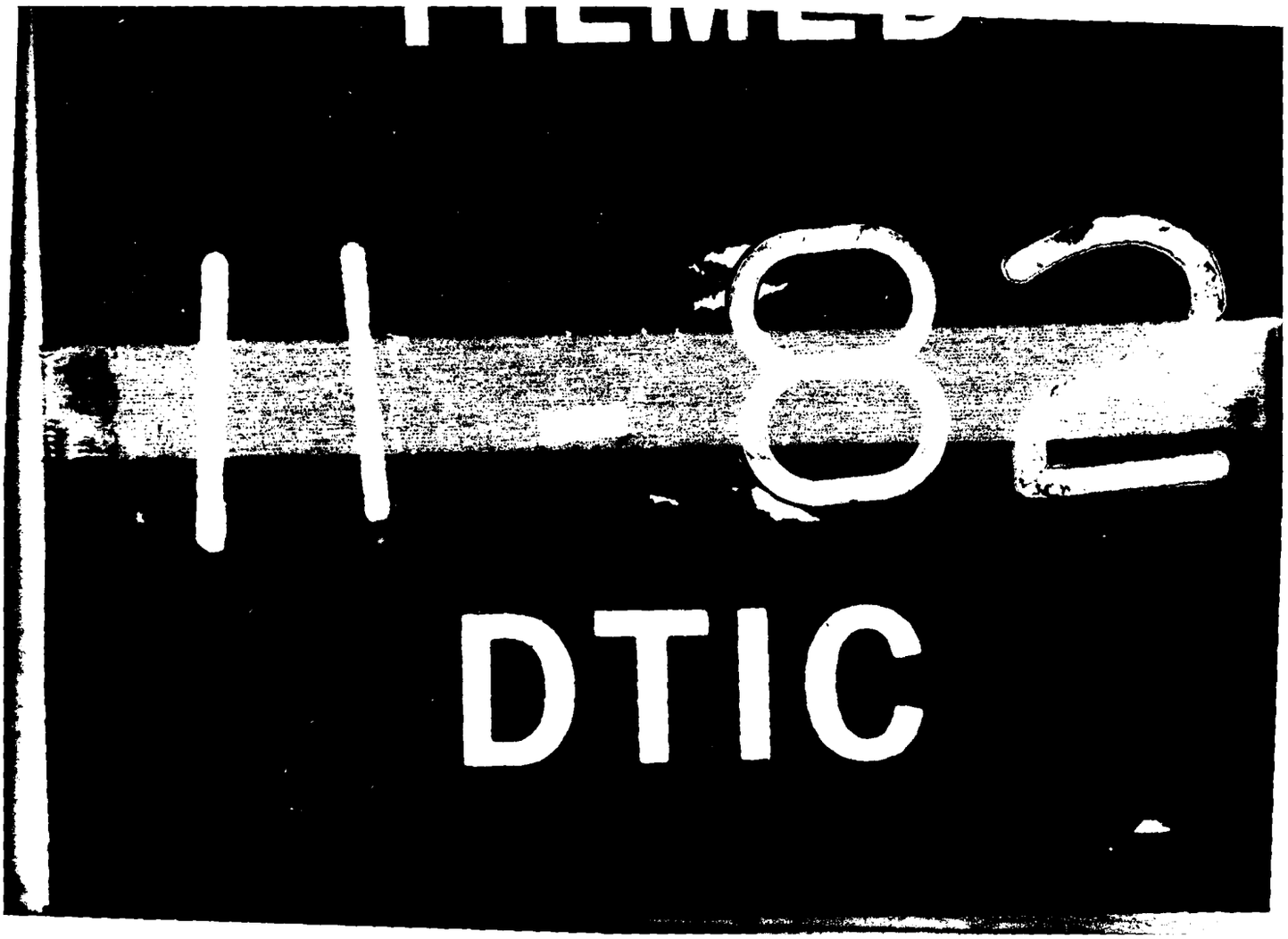
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